Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1. (Currently Amended) A disk controller comprising:

a channel adapter having ~~a~~ connection interfaces, to each of which a host computer or a disk drivel is to be coupled;

a memory adapter for temporarily storing data to be transferred between a ~~said~~ host computer and a ~~said~~ disk drive;

a processor adapter for controlling operations of said channel adapter and said memory adapter; and

a switch adapter for configuring an inner network by interconnecting said channel adapter, said memory adapter and said processor adapter,

wherein each of adapters including said channel adapter, said memory adapter, said processor adapter and said switch adapter~~, each~~ includes a DMA controller for performing a communication protocol control of said inner network; and

packet multiplex communication is performed among ~~said~~ DMA controllers of said adapters.

2. (Currently Amended) A~~The~~ disk controller according to claim 1, wherein

each of said adapters ~~said channel adapter, said memory adapter, said processor adapter and said switch adapter each~~ includes a plurality of DMA controllers and one or more data link engines; and

said plurality of DMA controllers share said one or more data link engines and perform DMA transfer at the same time via said one or more data link engines.

3-7. (Canceled).

8. (Currently Amended) A disk controller comprising:

a channel adapter having ~~a~~ connection interfaces, to each of which a host computer or a disk drivel is to be coupled;

a memory adapter for temporarily storing data to be transferred between a ~~said~~ host computer and a ~~said~~ disk drive;

a processor adapter for controlling operations of said channel adapter and said memory adapter; and

a switch adapter for configuring an inner network by interconnecting said channel adapter, said memory adapter and said processor adapter,

wherein each of adapters including said channel adapter, said memory adapter, said processor adapter and said switch adapter, ~~each~~ includes a DMA controller for performing a communication protocol control of said inner network;

a packet to be transferred among ~~said~~ DMA controllers of said adapters ~~provided in said adapters~~ has an address field for designating a targeting DMA controller, an address field for designating an initiating DMA controller and a DMA sequence field for managing a transfer order when one DMA transfer is divided into a plurality of packets; and

said DMA sequence field has a task ID unique to one DMA transfer.

9. (Currently Amended) A~~The~~ disk controller according to claim 8,

wherein a packet to be transferred among said DMA controllers of ~~provided~~ in said adapters has a first address for designating a relay DMA controller of said packet, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers.

10. (Currently Amended) A~~The~~ disk controller according to claim 9, wherein:

each of said adapters ~~said channel adapter, said memory adapter, said processor adapter and said switch adapter each~~ includes a plurality of DMA controllers and one or more data link engines;

a packet to be transferred among said DMA controllers of ~~provided in~~ said adapters comprises a routing field containing control information for a ~~said~~ data link engine, a command field containing control information for a ~~said~~ DMA controller and data field containing other data; and

said routing field includes a routing field error check code for checking a transfer error in said routing field, said command field includes a command field error check code for checking a transfer error in said command field, and said data field includes a data field error check code for checking a transfer error in said data field.

11. (Currently Amended) A~~The~~ disk controller according to claim 8, wherein

each of said adapters ~~said channel adapter, said memory adapter, said processor adapter and said switch adapter each~~ includes a plurality of DMA controllers and one or more data link engines;

a packet to be transferred among said DMA controllers of ~~provided in~~ said adapters comprises a routing field containing control information for a ~~said~~ data link engine, a command field containing control information for a ~~said~~ DMA controller and data field containing other data; and

said routing field includes a routing field error check code for checking a transfer error in said routing field, said command field includes a command field error check code for checking a transfer error in said command field, and said data field includes a data field error check code for checking a transfer error in said data field.

12. (Currently Amended) ~~The~~ A disk controller according to claim 11, wherein:

DMA sub-transfer is performed from a DMA controller designated by said initiating address field to a DMA controller designated by said targeting address field;

said DMA controller designated by said targeting address field returns a completion sub-status corresponding to said DMA sub-transfer to said DMA controller designated by said initiating address field;

said completion sub-status includes information of said DMA sequence field contained in said DMA sub-transfer; and

said DMA controller designated by said initiating address field confirms the information of said DMA sequence field contained in said completion sub-status to thereby confirm a transfer sequence of said DMA sub-transfer.

13. (Currently Amended) ~~The~~A disk controller according to claim 8, wherein:

DMA sub-transfer is performed from a DMA controller designated by said initiating address field to a DMA controller designated by said targeting address field;

said DMA controller designated by said targeting address field returns a completion sub-status corresponding to said DMA sub-transfer to said DMA controller designated by said initiating address field;

said completion sub-status includes information of said DMA sequence field contained in said DMA sub-transfer; and

said DMA controller designated by said initiating address field confirms the information of said DMA sequence field contained in said completion sub-status to thereby confirm a transfer sequence of said DMA sub-transfer.

14. (Currently Amended) ~~The~~A disk controller according to claim 9, wherein:

DMA sub-transfer is performed from a DMA controller designated by said initiating address field to a DMA controller designated by said targeting address field;

said DMA controller designated by said targeting address field returns a completion sub-status corresponding to said DMA sub-transfer to said DMA controller designated by said initiating address field;

said completion sub-status includes information of said DMA sequence field contained in said DMA sub-transfer; and

said DMA controller designated by said initiating address field confirms the information of said DMA sequence field contained in said completion sub-status to thereby confirm a transfer sequence of said DMA sub-transfer.

15. (Currently Amended) ~~The~~A disk controller according to claim 14, wherein:

if a packet to be transferred among said DMA controllers has a first address for designating said DMA controller in said switch adapter, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers;

said DMA controller in said switch adapter generates a packet which has said second address in said targeting address field and contains said transfer data and a packet which has said third address in said targeting address field and contains said transfer data.

16. (Currently Amended) ~~The~~A disk controller according to claim 8, wherein:

if a packet to be transferred among said DMA controllers has a first address for designating said DMA controller in said switch adapter, second and third

addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers;

said DMA controller in said switch adapter generates a packet which has said second address in said targeting address field and contains said transfer data and a packet which has said third address in said targeting address field and contains said transfer data.

17. (Currently Amended) ~~The~~A ~~-~~disk controller according to claim 9, wherein:

if a packet to be transferred among said DMA controllers has a first address for designating said DMA controller in said switch adapter, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers;

said DMA controller in said switch adapter generates a packet which has said second address in said targeting address field and contains said transfer data and a packet which has said third address in said targeting address field and contains said transfer data.

18. (Currently Amended) ~~The~~A ~~-~~disk controller according to claim 10, wherein:

if a packet to be transferred among said DMA controllers has a first address for designating said DMA controller in said switch adapter, second and third addresses for designating targeting DMA controllers, and transfer data to be transferred to said targeting DMA controllers;

said DMA controller in said switch adapter generates a packet which has said second address in said targeting address field and contains said transfer data and a

packet which has said third address in said targeting address field and contains said transfer data.

19. (Currently Amended) A~~The~~ disk controller according to claim 8, wherein

a packet to be transferred among said DMA controllers of ~~provided in~~ said adapters comprises a header field containing packet control information and a data field containing other data;

said header field includes a header field error check code for checking a transfer error in said header field, and said data field includes a data field error check code for checking a transfer error in said data field; and

said DMA controller in said switch adapter passes only a packet having a correct header field error check code.

20. (Currently Amended) A~~The~~ disk controller according to claim 9, wherein

a packet to be transferred among said DMA controllers of ~~provided in~~ said adapters comprises a header field containing packet control information and a data field containing other data;

said header field includes a header field error check code for checking a transfer error in said header field, and said data field includes a data field error check code for checking a transfer error in said data field; and

said DMA controller in said switch adapter passes only a packet having a correct header field error check code.

21. (Currently Amended) A~~The~~ disk controller according to claim 1, wherein;

each of said adapters ~~said channel adapter, said memory adapter, said processor adapter and said switch adapter each~~ includes a plurality of DMA controllers and a plurality of data link engines; and

when a~~said~~ DMA controller performs DMA transfer via a~~said~~ data link engine, said DMA transfer is performed via an identical ~~same~~ data line engine during one DMA transfer.

21-24. (Canceled).